EP 0 971 359 A2

FIG.1

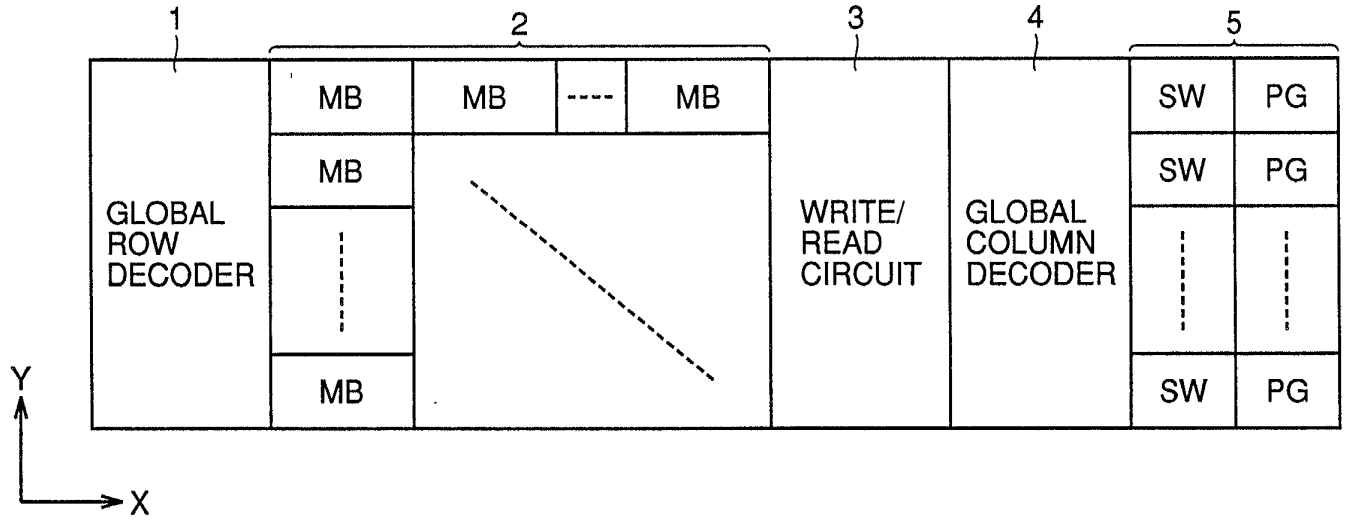


FIG.2

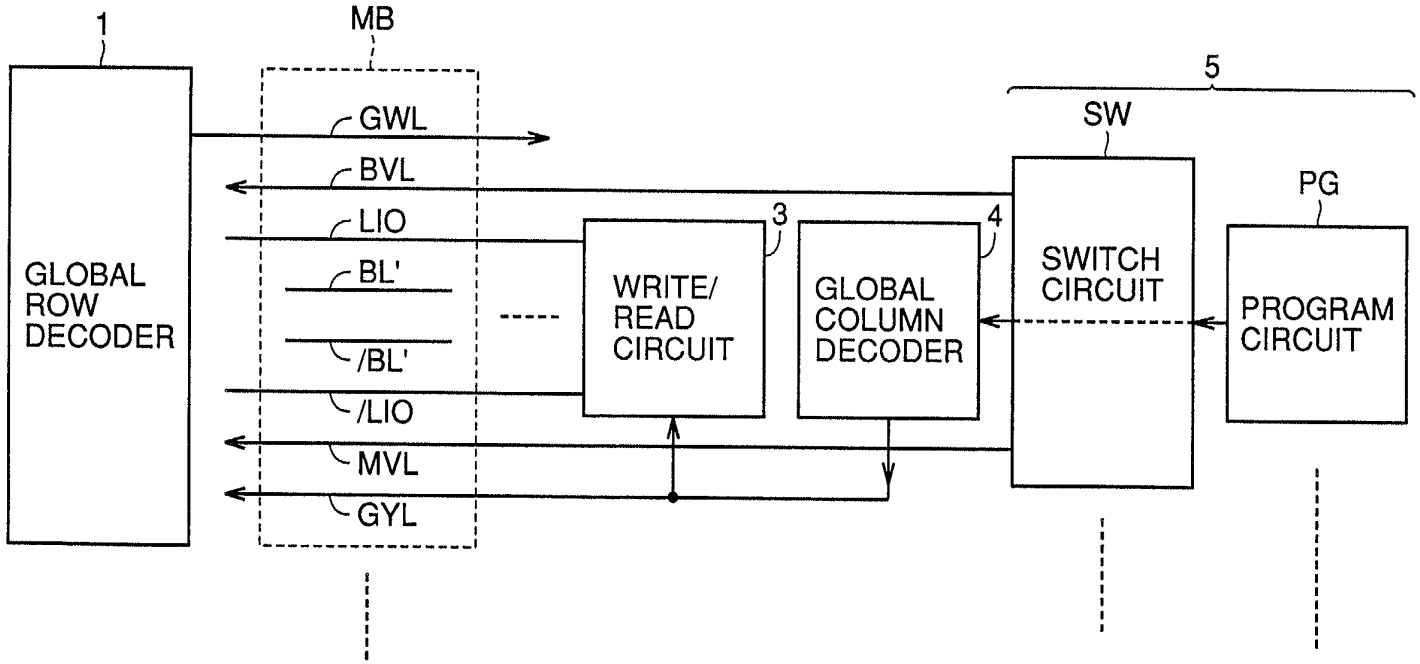

1
MB
5
SW
PG
GWL
BVL
LIO
BL'
/BL'
/LIO
MVL
GYL
GLOBAL ROW DECODER
WRITE/ READ CIRCUIT
3
GLOBAL COLUMN DECODER
4
SWITCH CIRCUIT
PROGRAM CIRCUIT

FIG.3

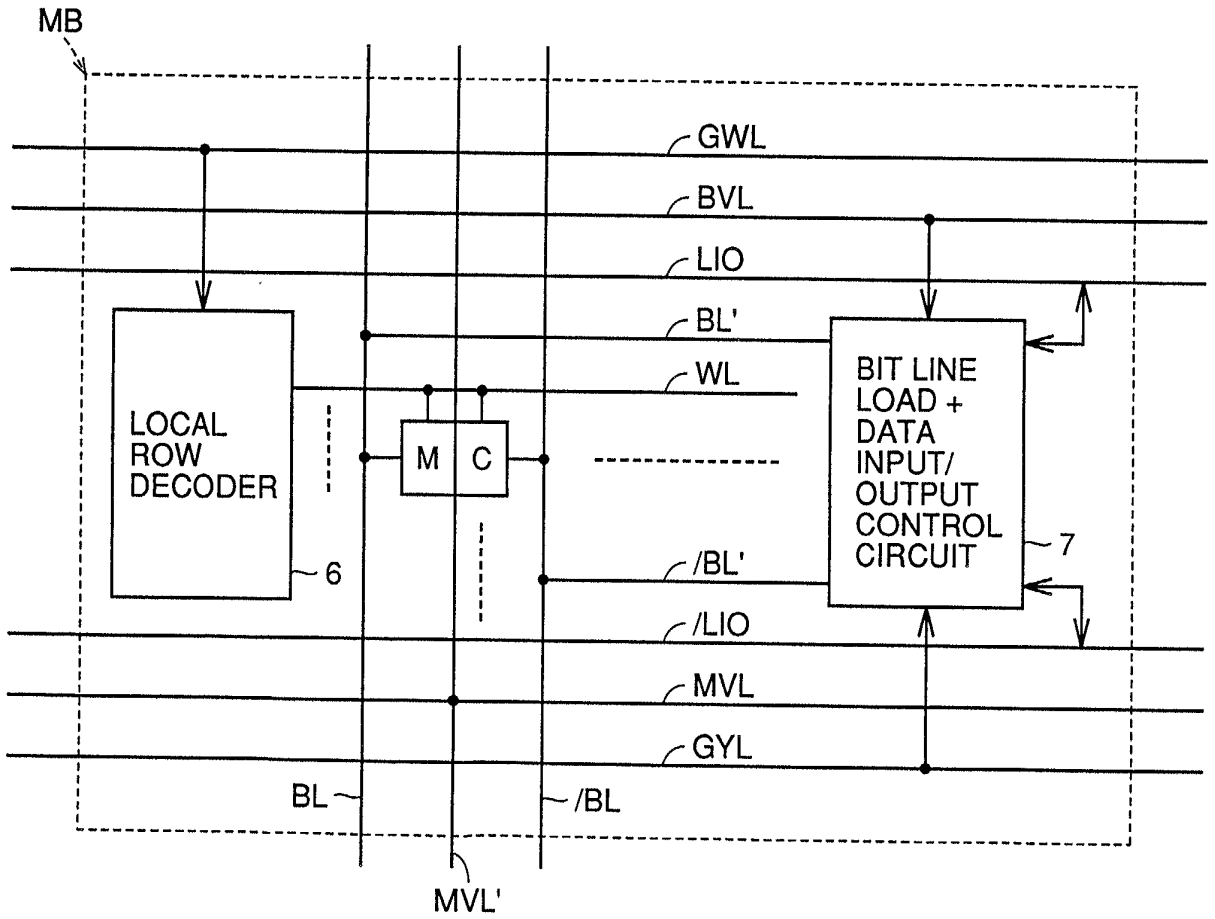

MB
GWL
BVL
LIO
BL'
WL
LOCAL ROW DECODER
6
M
C
BIT LINE LOAD + DATA INPUT/ OUTPUT CONTROL CIRCUIT
7
/BL'
/LIO
MVL
GYL
BL
/BL
MVL'

FIG.4A

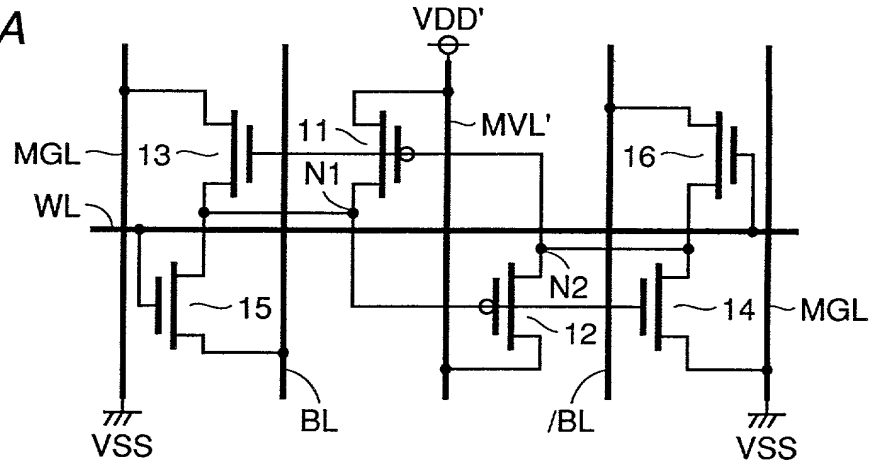


FIG.4B

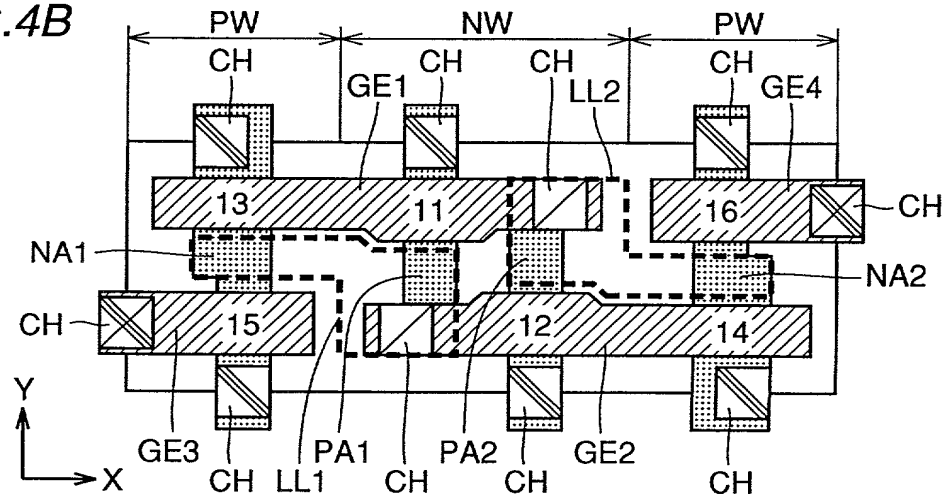


FIG.4C

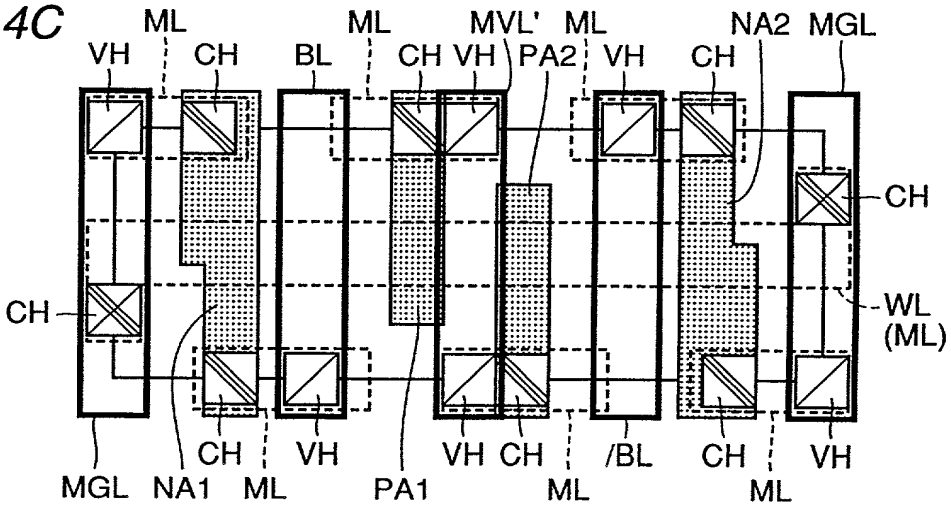


FIG.5

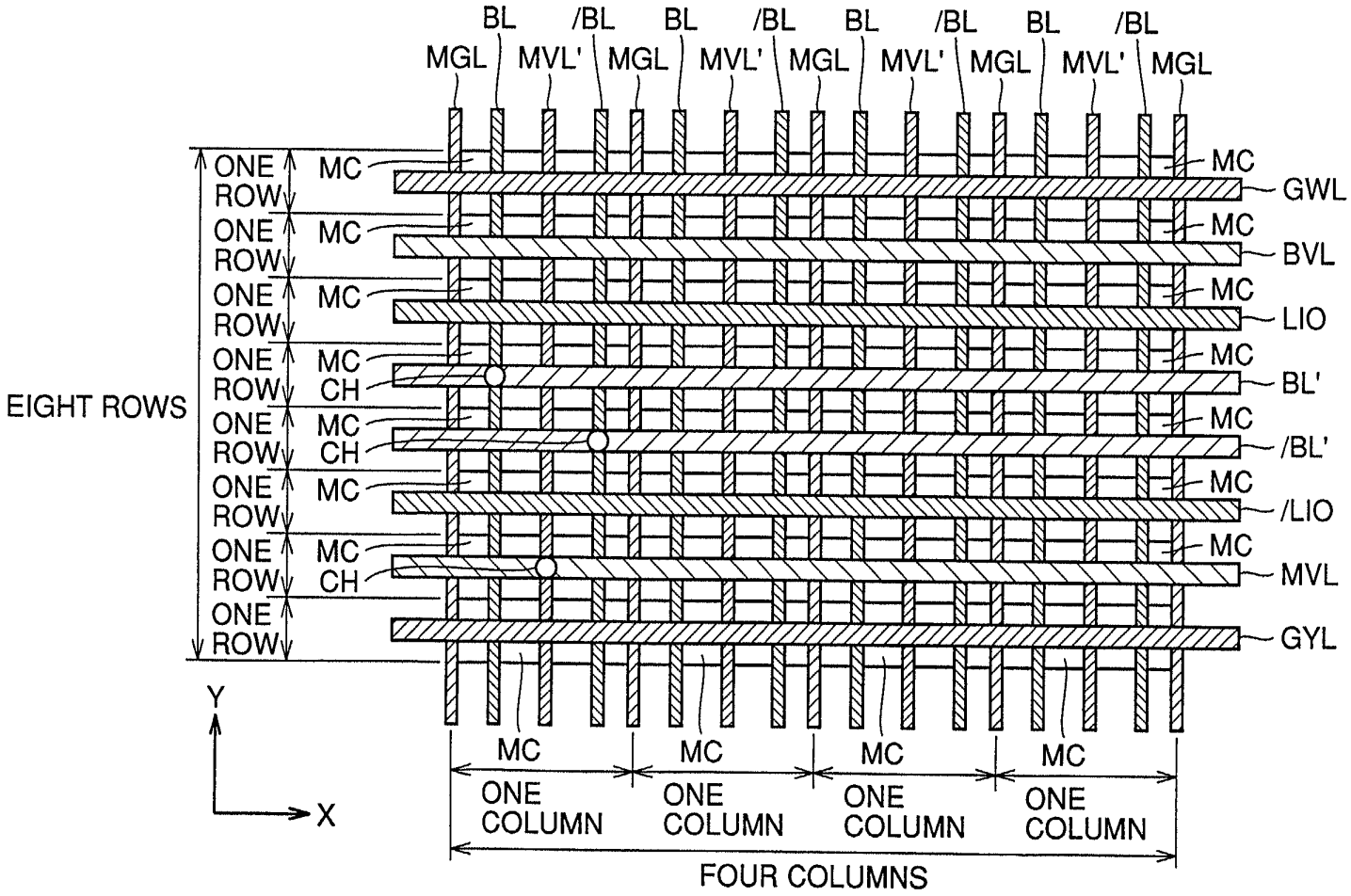

BL
/BL
MGL
MVL'
MC
GWL
BVL
LIO
BL'
/BL'
/LIO
MVL
GYL
CH
ONE ROW
EIGHT ROWS
Y
X
ONE COLUMN
FOUR COLUMNS

FIG.6

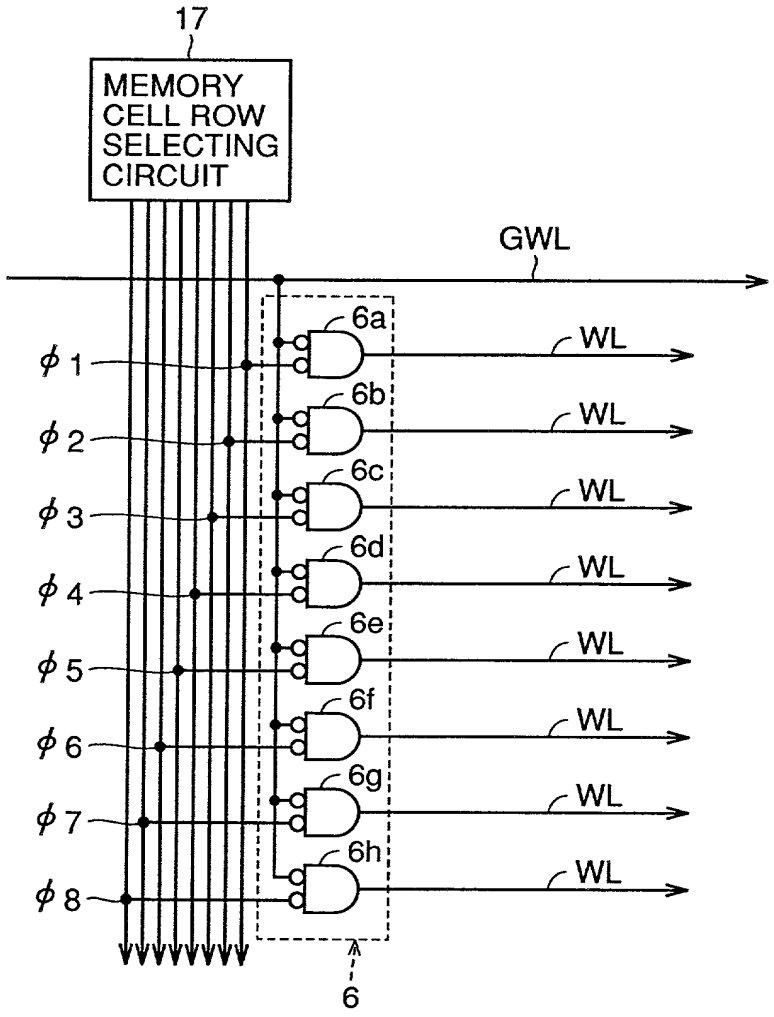

17
MEMORY CELL ROW SELECTING CIRCUIT
GWL
φ1
φ2
φ3
φ4
φ5
φ6
φ7
φ8
6a
6b
6c
6d
6e
6f
6g
6h
WL
WL
WL
WL
WL
WL
WL
WL
6

FIG.7

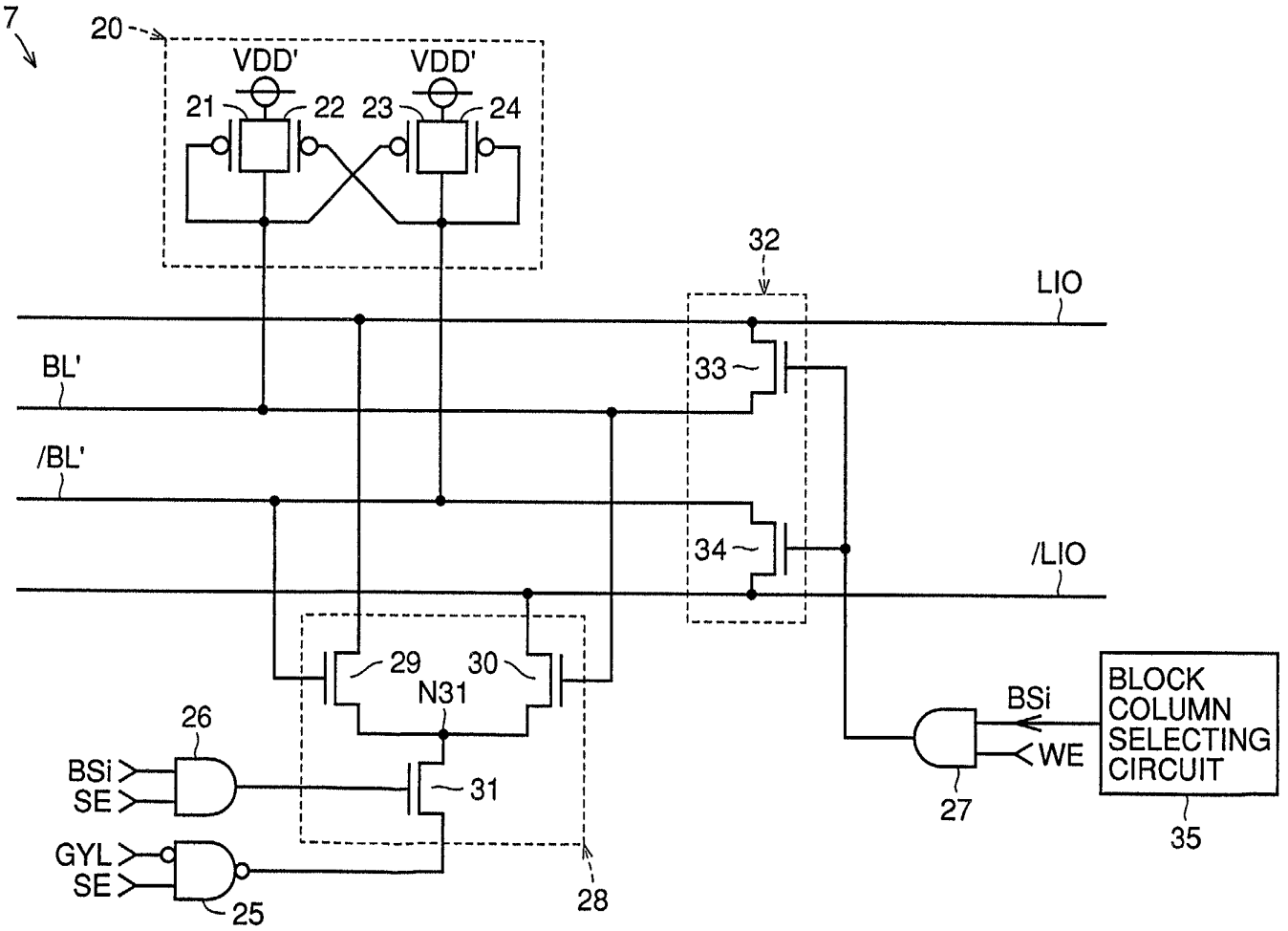

7
20
VDD'
VDD'
21
22
23
24
32
LIO
BL'
33
/BL'
34
/LIO
29
30
N31
26
BSi
SE
31
GYL
SE
25
28
BSi
WE
27
BLOCK
COLUMN
SELECTING
CIRCUIT
35

FIG.8

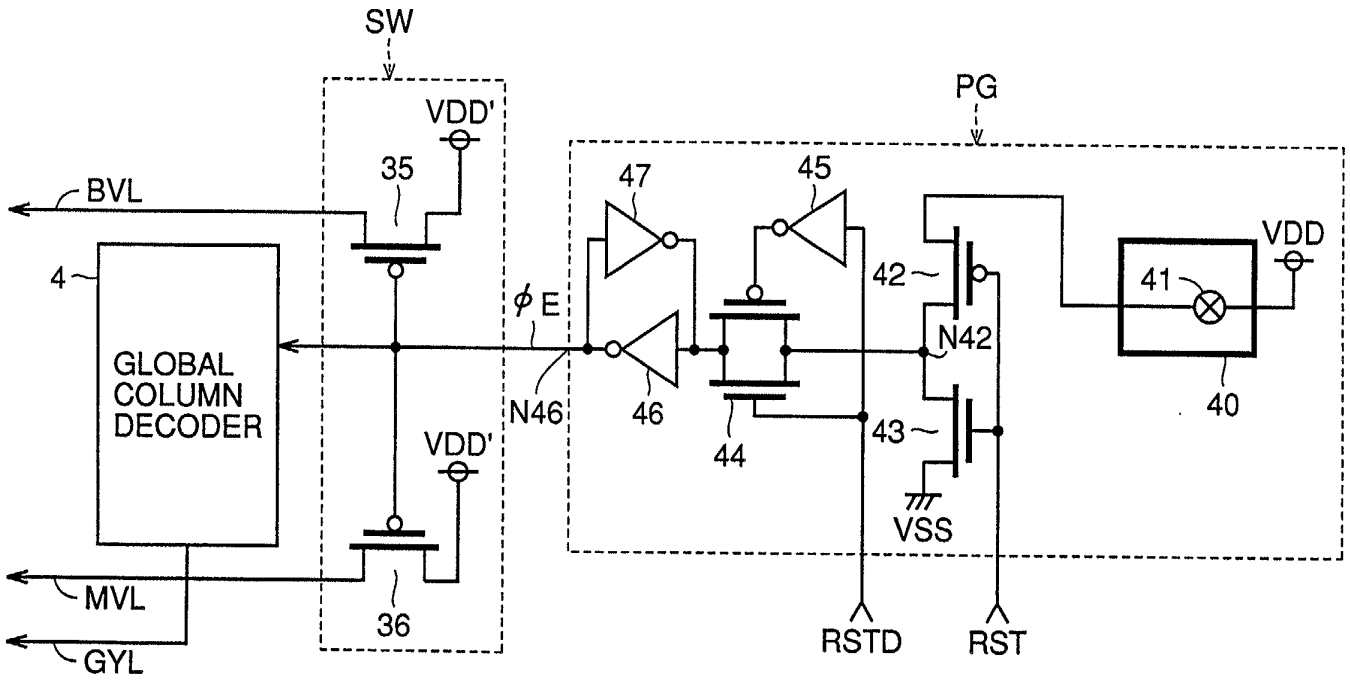

SW
PG
VDD'
35
BVL
4
GLOBAL
COLUMN
DECODER
φE
N46
47
46
45
44
42
N42
43
VSS
VDD
41
40
VDD'
36
MVL
GYL
RSTD
RST

FIG.9

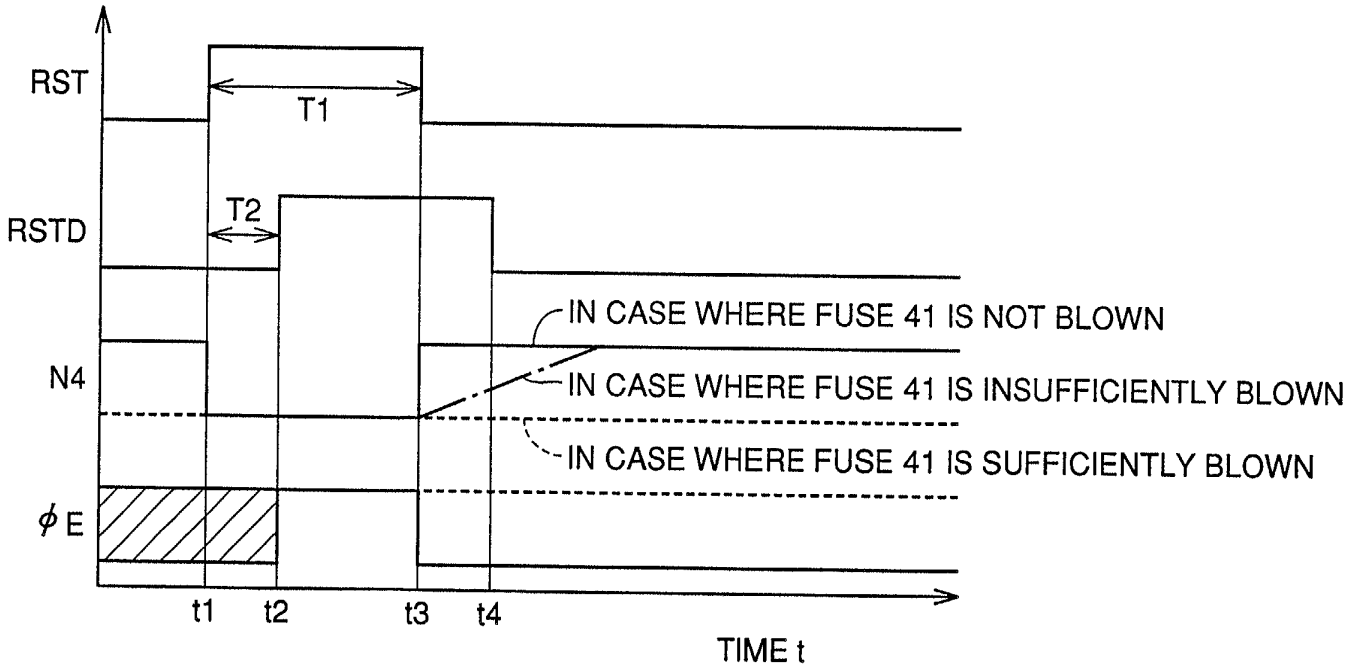

RST
T1
RSTD
T2
IN CASE WHERE FUSE 41 IS NOT BLOWN
N4
IN CASE WHERE FUSE 41 IS INSUFFICIENTLY BLOWN
IN CASE WHERE FUSE 41 IS SUFFICIENTLY BLOWN
φE
t1
t2
t3
t4
TIME t

FIG.10

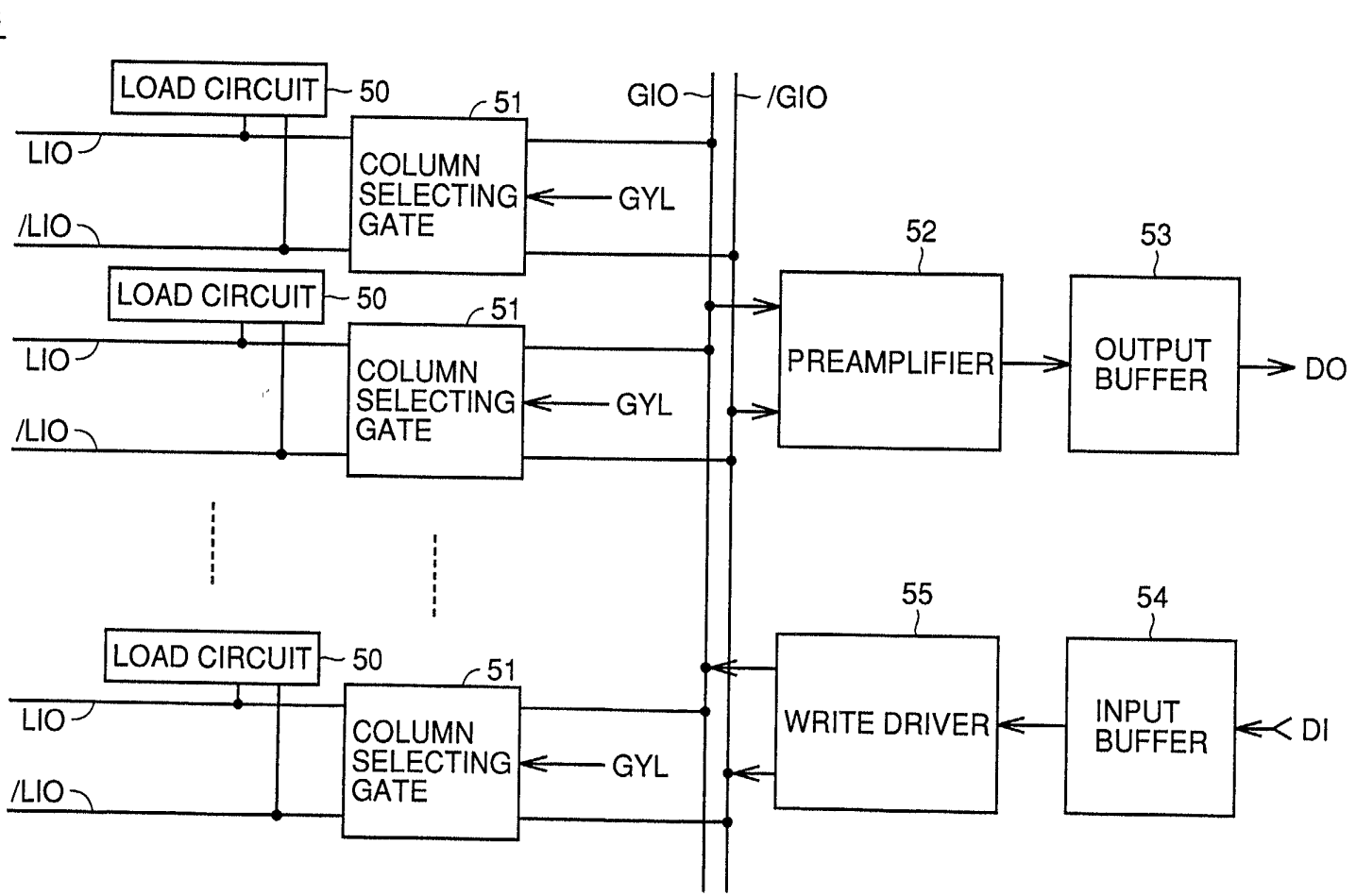
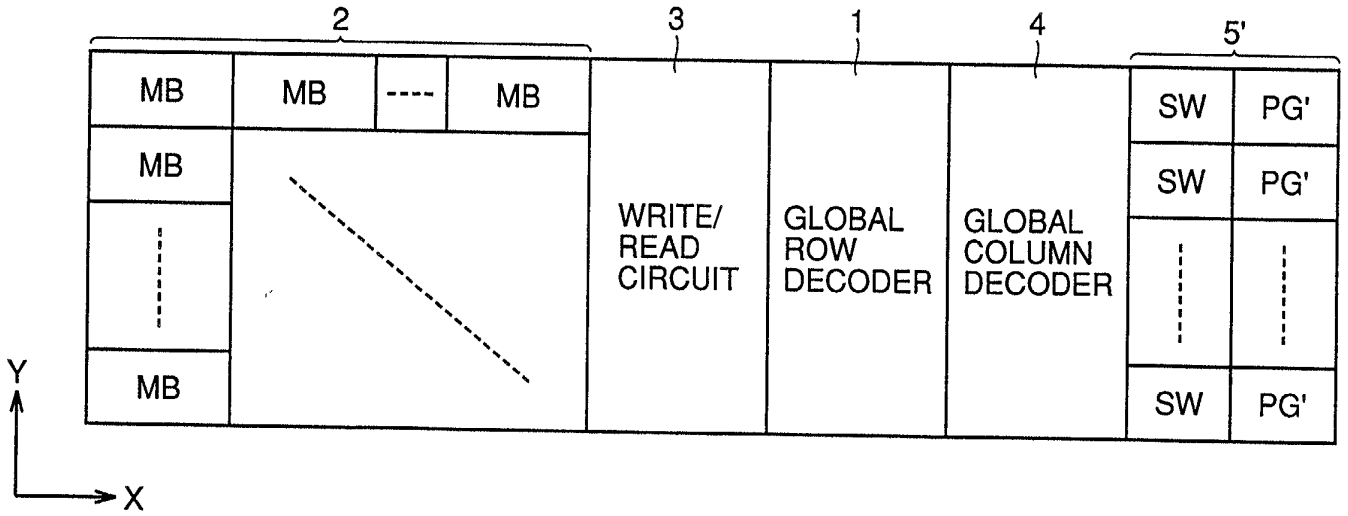

3
LOAD CIRCUIT
50
51
GIO
/GIO
LIO
/LIO
COLUMN SELECTING GATE
GYL
52
53
PREAMPLIFIER
OUTPUT BUFFER
DO
55
54
WRITE DRIVER
INPUT BUFFER
DI

FIG.11


2
3
1
4
5'
MB
MB

MB
MB
MB
WRITE/
READ
CIRCUIT
GLOBAL
ROW
DECODER
GLOBAL
COLUMN
DECODER
SW
PG'
SW
PG'
SW
PG'
Y
X

FIG.12

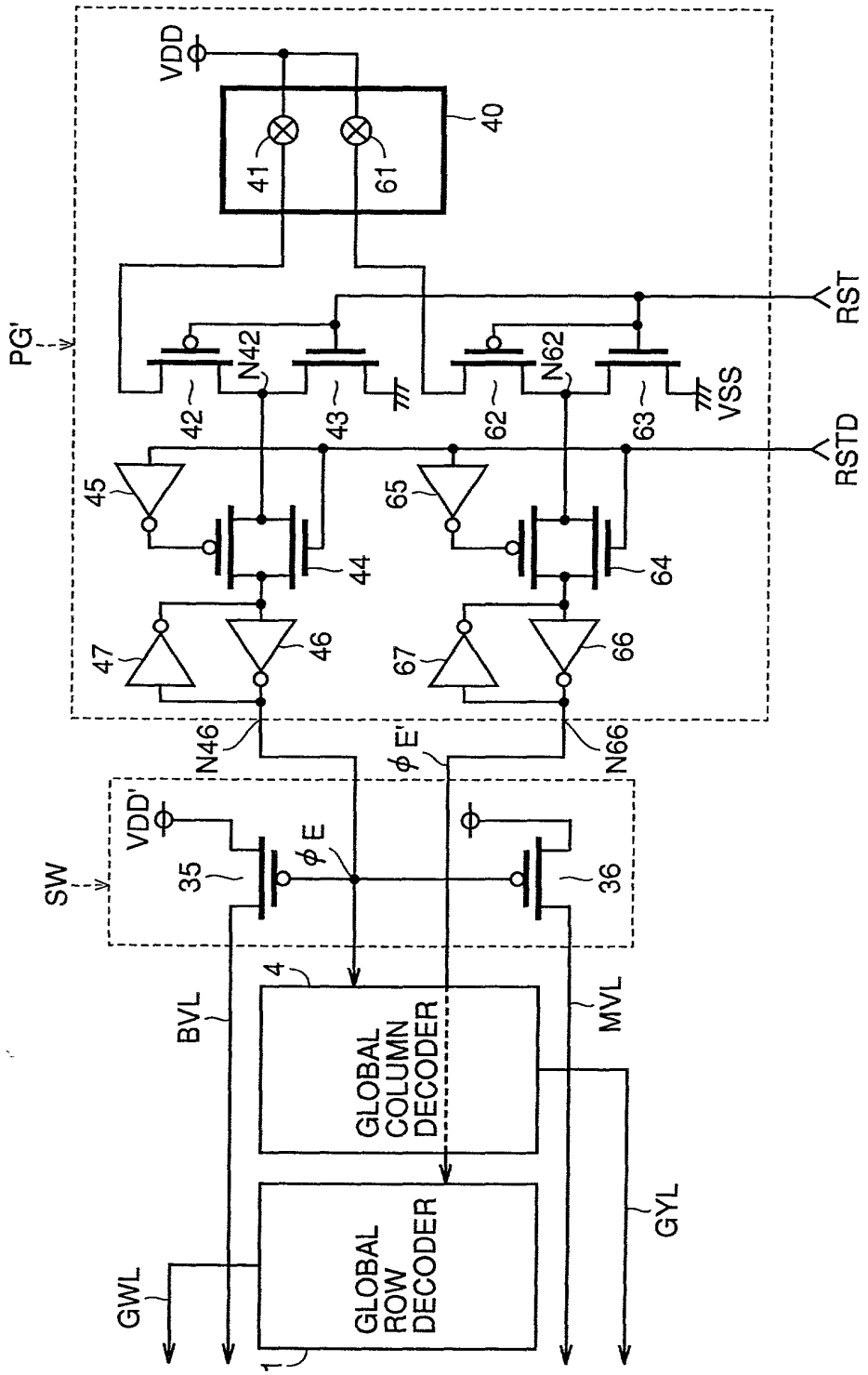

VDD
40
41
61
PG'
N42
N62
RST
RSTD
VSS
42
43
62
63
45
65
44
64
47
67
46
66
N46
N66
φE'
SW
VDD'
φE
35
36
4
BVL
MVL
GLOBAL COLUMN DECODER
GLOBAL ROW DECODER
GWL
GYL
1

FIG.13A PRIOR ART

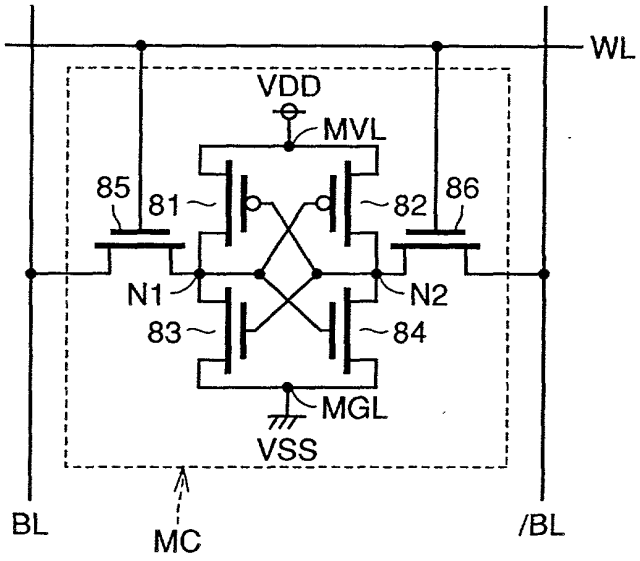


FIG.13B PRIOR ART

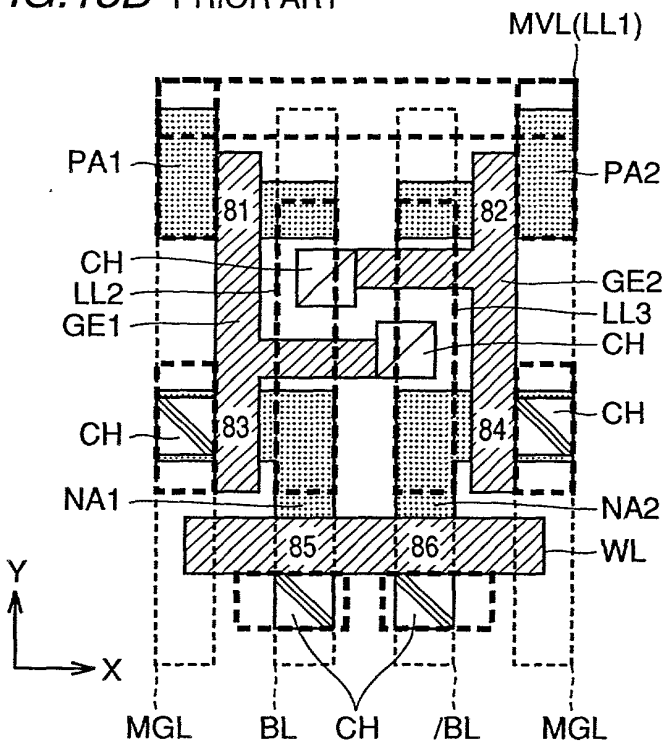


FIG.14A PRIOR ART

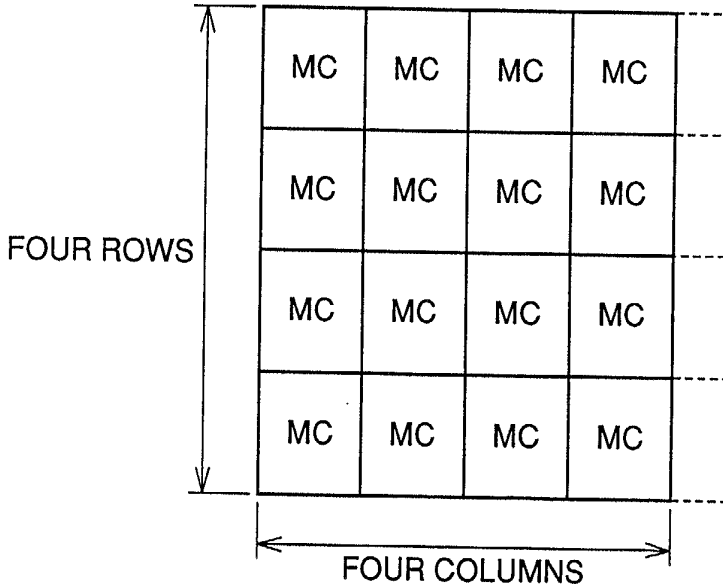
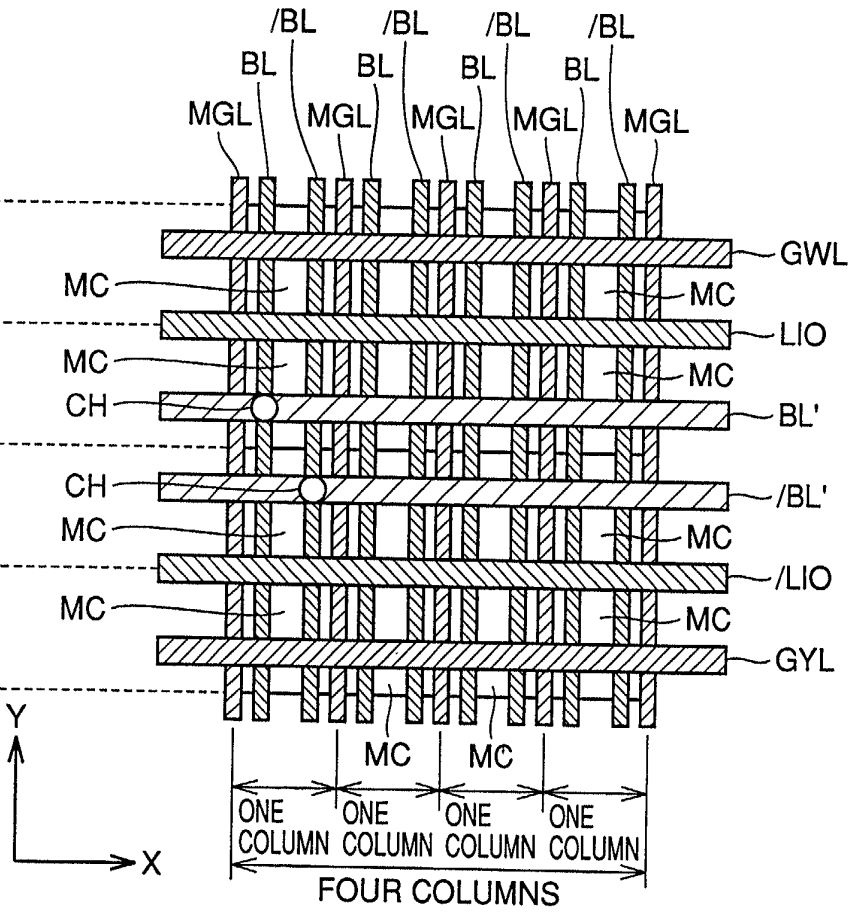



FIG.14B PRIOR ART